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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,763	12/02/2003	Shin Kikuchi	03500.017750	1799

5514 7590 04/12/2007

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
HSU, AMY R	
ART UNIT	**PAPER NUMBER**
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/724,763	KIKUCHI, SHIN	
	Examiner	Art Unit	
	Amy Hsu	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/30/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Objections

1. Claim 1 is objected to because of the following informalities: "filed" describing the field effect transistor should be changed to "field". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirota (US 6,084,273).

Regarding Claim 1, Hirota teaches a photoelectric conversion device (*taught in the imaging device in Fig. 7)* comprising: a photoelectric conversion region for accumulating electric charges that correspond to incident light (the photodiode depicted by *Fig. 8 reference number 42 and Col 8 Lines 45-48.)*; and an amplifying filed effect transistor (*Fig. 24 and Col 6 Lines 9-12)* into which a signal charge from the photoelectric conversion region is inputted (*Fig. 10 shows the input from the photoelectric conversion region, reference number 86, being inputted to the FET)*, wherein: the photoelectric conversion region is surrounded by a potential barrier region *(the photodiode pictured on the extreme left side of Fig. 8 is surrounded by a potential barrier region denoted by reference numbers 52 and 56 and into 49)* ; a nick region is

formed in a part of the potential barrier region (*Fig. 8 between reference numbers 50 and 54 which acts as an overflow channel region)*; and one of main electrode regions of the field effect transistor is placed adjacent to the nick region (*the electrode region of the FET, Fig. 10 reference number 81, lies close, or adjacent, to the nick region between the two photodiodes of reference number 86*), the main electrode region having the same conductivity type as the photoelectric conversion region (*the main electrode region has n+ conductivity as shown in Fig. 10 number 81, as does the photodiode as pictured in Fig. 8 number 50*).

Note: For purposes of examining, a nick region is characterized as an overflow channel region as described in applicant's disclosure in paragraph 29.

Regarding Claim 2, Hirota teaches a photoelectric conversion device according to claim 1, wherein the potential barrier region includes at least a selectively oxidized film and a channel stopping layer directly below the selectively oxidized film (*Fig. 8 reference number 56 and Col 8 Line 51 describe a silicon oxide film with a channel stopping region, Fig 8 reference number 52 and Col 8 Line 55, directly below 56).*

Regarding Claim 3, Hirota teaches a photoelectric conversion device according to claim 1, wherein the potential barrier region includes at least a buried isolation region (*Fig. 8 reference number 52 and the space below it with p type conductivity*) whose conductivity type is opposite to that of the photoelectric conversion region (*Fig. 8 reference number 50 with opposite, or n type, conductivity*).

Regarding Claim 4, Hirota teaches a photoelectric conversion device according to claim 1, wherein the photoelectric conversion region is formed in a low impurity

concentration region (*Fig 8. reference number 49 which is p type conductivity*) that is doped with an impurity of the same conductivity type as the photoelectric conversion region (*Fig. 8 reference number 53, also p type*) in a concentration lower than the impurity concentration of the photoelectric conversion region (*the p well in the pn junction comprising the photodiode or photoelectric conversion region, Fig. 8 reference number 42, has a material denoted by P++, as opposed to the region it is formed in, 49, denoted by P. The material denoted by P inherently has a lower impurity concentration than the material denoted by P++).*

Regarding Claim 5, Hirota teaches a photoelectric conversion device according to claim 4, wherein a buried isolation region (*Fig. 8 reference number 52 into reference number 49, both with p type conductivity*) whose conductivity type is opposite to the conductivity type of the photoelectric conversion region (*Fig. 8 reference number 50 of n type*) is formed below the field effect transistor (*49 forms below the FET because the FET is forms at the top of 49 as seen in Fig. 9 and does not extend to the bottom of 49*).

Note: Since the applicant's disclosure does not specifically define or further limit the buried isolation region, then the buried isolation region is best depicted by applicant's Fig. 1B at the dotted line region of the potential barrier in reference number 12. This buried isolation region is the area between the channel stopper and the p well, reference number 4. This same area is found in Hirota's Fig. 8 below the channel stopping region 52, which is into 49, with identical conductivity as applicant's disclosure and is therefore the same buried isolation region as applicant discloses.

Regarding Claim 6, Hirota teaches a photoelectric conversion device according to claim 5, wherein the buried isolation region placed below the field effect transistor (Fig. 8, the area within 49 below 52) surrounds a region larger than the photoelectric conversion region (49 is larger than 42), and wherein the region surrounded by the buried isolation region functions as a photosensitive region *(42, the photodiode, also depicted by the p-n junction on the extreme left of Fig. 8 is surrounded by 49 the buried isolation region, where the photodiode functions as a photosensitive region as described in Col 8 Lines 36-37).*

Regarding Claim 7, Hirota teaches a photoelectric conversion device according to claim 1, wherein an impurity diffusion region (*Fig. 8 reference number 49 of p type conductivity*) whose conductivity type is opposite to the conductivity type of the photoelectric conversion region (*Fig. 8 number 50 of n type conductivity*) is provided in the nick region (*within 49*).

Regarding Claim 8, Hirota teaches a photoelectric conversion device according to claim 5, wherein the buried isolation region is not placed in an area below the one main electrode region of the field effect transistor, at least, a part of the area (*the buried isolation region, part of which is represented by Fig. 8 reference number 52, is not placed in an area below the main electrode of the FET because the FET as depicted in Fig. 9 reference number 81 is at the top of 49 and 52 is also on the top of 49, showing that the buried isolation region is on the same level as the FET and not below it*).

Regarding Claim 9, Hirota teaches a photoelectric conversion device according to claim 1, wherein the potential barrier region (*Fig. 8 including reference numbers 56, 52, and into 49*) includes at least a semiconductor region whose conductivity type (*52 with p type*) is opposite to the conductivity type of the photoelectric conversion region (*50 with n type*), and wherein a buried region (*Fig. 8 the area of 49 just under 52 as noted above in the paragraph regarding Claim 5*) that is doped with an impurity of the same conductivity type as the semiconductor region (*both buried region and semiconductor region are p type*) in a concentration lower than the impurity concentration of the semiconductor region (*Fig. 8 number 52*) is placed in the nick region (*within Fig. 8 number 49 region*).

Note: Impurity concentration is inherently lower in regions farther from the surface. Therefore the impurity concentration of the buried region, which is deeper into the surface will be lower than the concentration of the semiconductor region, which is closer to the surface.

Regarding Claim 10, Hirota teaches a photoelectric conversion device according to claim 4, wherein the low impurity concentration region is one of a semiconductor substrate, an epitaxial layer, and a well (*Fig. 8 reference number 49 is a semiconductor substrate*).

Regarding Claim 11, Hirota teaches a photoelectric conversion device according to claim 1, wherein the one main electrode region (*Fig. 10 reference number 81*) is connected to a fixed electric potential or a similar electric potential (*power supply voltage as described in Col 9 Lines 46-49*).

Regarding Claim 12, Hirota teaches a photoelectric conversion device according to claim 1, wherein a semiconductor region (*Fig. 8 reference number 49 of p conductivity type*) whose conductivity type is opposite to the conductivity type of the photoelectric conversion region (*Fig. 8 reference number 50 of n type*) is placed below the photoelectric conversion region (*49 being below 50*).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirota (US 6,084,273).

Regarding Claim 13, Hirota teaches a photoelectric conversion device according to claim 1. It would be obvious to one of ordinary skill in the art at the time the invention was made to combine a standard image pick-up system with an optical system for forming an image in the photoelectric conversion device; and a signal processing circuit for processing a signal outputted from the photoelectric conversion device with the photoelectric conversion device taught by Hirota because the function of the photoelectric conversion device is optimally utilized commercially within an image pickup system.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure including Yang (US 6180969), Toma (US 6778214), Kawamoto et al. (US 5831298), Surisawa et al. (US 6215521), Inagaki (US 6765246), Zhao (US 6586789).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amy Hsu whose telephone number is 571-270-3012. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 571-272-7331. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amy Hsu
Examiner
Art Unit 2609

ah

CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600